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UTILITY PATENT APPLICATION TRANSMITTAL

(Only for new nonprovisional applications under 37 C.F.R. § 1.53(b))

Attorney Docket No. RCA 89,324 / PU000125

First Inventor or Application Identifier Horlander et.al.

Title SERIAL COMPRESSED BUS *

Express Mail Label No. EL555972980US

APPLICATION ELEMENTS

See MPEP chapter 600 concerning utility patent application contents.

1. * Fee Transmittal Form (e.g., PTO/SB/17)
(Submit an original and a duplicate for fee processing)
2. Specification [Total Pages 10]
(preferred arrangement set forth below)
 - Descriptive title of the Invention
 - Cross References to Related Applications
 - Statement Regarding Fed sponsored R & D
 - Reference to Microfiche Appendix
 - Background of the Invention
 - Brief Summary of the Invention
 - Brief Description of the Drawings (if filed)
 - Detailed Description
 - Claim(s)
 - Abstract of the Disclosure
3. Drawing(s) (35 U.S.C. 113) [Total Sheets 3]
4. Oath or Declaration [Total Pages]
 - a. Newly executed (original or copy)
 - b. Copy from a prior application (37 C.F.R. § 1.63(d))
(for continuation/divisional with Box 16 completed)
 - i. DELETION OF INVENTOR(S)
Signed statement attached deleting inventor(s) named in the prior application, see 37 C.F.R. §§ 1.63(d)(2) and 1.33(b).

*NOTE FOR ITEMS 1 & 13: IN ORDER TO BE ENTITLED TO PAY SMALL ENTITY FEES, A SMALL ENTITY STATEMENT IS REQUIRED (37 C.F.R. § 1.27), EXCEPT IF ONE FILED IN A PRIOR APPLICATION IS RELIED UPON (37 C.F.R. § 1.28).

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5. Microfiche Computer Program (Appendix)
6. Nucleotide and/or Amino Acid Sequence Submission
(if applicable, all necessary)
 - a. Computer Readable Copy
 - b. Paper Copy (identical to computer copy)
 - c. Statement verifying identity of above copies

ACCOMPANYING APPLICATION PARTS

7. Assignment Papers (cover sheet & document(s))
8. 37 C.F.R. § 3.73(b) Statement Power of (when there is an assignee) Attorney
9. English Translation Document (if applicable)
10. Information Disclosure Statement (IDS)/PTO-1449 2 Copies of IDS Citations
11. Preliminary Amendment
12. Return Receipt Postcard (MPEP 503)
(Should be specifically itemized)
13. * Small Entity Statement(s) Statement filed in prior application, (PTO/SB/09-12) Status still proper and desired
14. Certified Copy of Priority Document(s)
(if foreign priority is claimed)
15. Other:

16. If a CONTINUING APPLICATION, check appropriate box, and supply the requisite information below and in a preliminary amendment:

Continuation Divisional Continuation-in-part (CIP) of prior application No: _____

Prior application information: Examiner _____ Group / Art Unit: _____

For CONTINUATION or DIVISIONAL APPS only: The entire disclosure of the prior application, from which an oath or declaration is supplied under Box 4b, is considered a part of the disclosure of the accompanying continuation or divisional application and is hereby incorporated by reference. The incorporation can only be relied upon when a portion has been inadvertently omitted from the submitted application parts.

17. CORRESPONDENCE ADDRESS

<input type="checkbox"/> Customer Number or Bar Code Label	(Insert Customer No. or Attach bar code label here)			<input type="checkbox"/> Correspondence address below	
Name	Joseph S. Tripoli Thomson Multimedia Licensing Inc.				
Address	Patent Operation Two Independence Way, P. O. Box 5312				
City	Princeton	State	NJ	Zip Code	08543-5312
Country	USA	Telephone	609/734- 9875	Fax	609/734-9700

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Signature			
	Date	20 Nov 2000	

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* INTERFACE HAVING A REDUCED PIN COUNT

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FEE TRANSMITTAL

for FY 2000

*Patent fees are subject to annual revision.**Small Entity payments must be supported by a small entity statement, otherwise large entity fees must be paid. See Forms PTO/SB/09-12. See 37 C.F.R. §§ 1.27 and 1.28.*

TOTAL AMOUNT OF PAYMENT (\$ 710.00)

Complete if Known

Application Number	
Filing Date	Herewith
First Named Inventor	Horlander et.al.
Examiner Name	
Group / Art Unit	
Attorney Docket No.	RCA89,324/PU000125

METHOD OF PAYMENT (check one)

1. The Commissioner is hereby authorized to charge indicated fees and credit any overpayments to:

Deposit Account Number 07-0832

Deposit Account Name THOMSON multimedia Licensing Inc.

 Charge Any Additional Fee Required Under 37 CFR §§ 1.16 and 1.17

2. Payment Enclosed:

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FEE CALCULATION

1. BASIC FILING FEE

Large Entity	Small Entity	Fee Code (\$)	Fee Code (\$)	Fee Description	Fee Paid
101 690	201 345	Utility filing fee		710.00	
106 310	206 155	Design filing fee			
107 480	207 240	Plant filing fee			
108 690	208 345	Reissue filing fee			
114 150	214 75	Provisional filing fee			
SUBTOTAL (1) (\$ 710.00)					

2. EXTRA CLAIM FEES

Total Claims	-20**	= 0	X	Fee from below	Fee Paid
Independent Claims	3	-3**	= 0	X	
Multiple Dependent					

** or number previously paid, if greater; For Reissues, see below

Large Entity Small Entity

Fee Code (\$)	Fee Code (\$)	Fee Description	Fee Paid
103 18	203 9	Claims in excess of 20	
102 78	202 39	Independent claims in excess of 3	
104 260	204 130	Multiple dependent claim, if not paid	
109 78	209 39	** Reissue independent claims over original patent	
110 18	210 9	** Reissue claims in excess of 20 and over original patent	
SUBTOTAL (2) (\$ 0)			

3. ADDITIONAL FEES

Large Entity	Small Entity	Fee Code (\$)	Fee Code (\$)	Fee Description	Fee Paid
105 130	205 65	Surcharge - late filing fee or oath			
127 50	227 25	Surcharge - late provisional filing fee or cover sheet			
139 130	139 130	Non-English specification			
147 2,520	147 2,520	For filing a request for reexamination			
112 920*	112 920*	Requesting publication of SIR prior to Examiner action			
113 1,840*	113 1,840*	Requesting publication of SIR after Examiner action			
115 110	215 55	Extension for reply within first month			
116 380	218 190	Extension for reply within second month			
117 870	217 435	Extension for reply within third month			
118 1,380	218 680	Extension for reply within fourth month			
128 1,850	228 925	Extension for reply within fifth month			
119 300	219 150	Notice of Appeal			
120 300	220 150	Filing a brief in support of an appeal			
121 260	221 130	Request for oral hearing			
138 1,510	138 1,510	Petition to institute a public use proceeding			
140 110	240 55	Petition to revive - unavoidable			
141 1,210	241 605	Petition to revive - unintentional			
142 1,210	242 605	Utility issue fee (or reissue)			
143 430	243 215	Design issue fee			
144 580	244 290	Plant issue fee			
122 130	122 130	Petitions to the Commissioner			
123 50	123 50	Petitions related to provisional applications			
128 240	128 240	Submission of Information Disclosure Stmt			
581 40	581 40	Recording each patent assignment per property (times number of properties)			
148 690	248 345	Filing a submission after final rejection (37 CFR § 1.129(a))			
149 690	249 345	For each additional invention to be examined (37 CFR § 1.129(b))			
Other fee (specify) _____					
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* Reduced by Basic Filing Fee Paid				SUBTOTAL (3) (\$)	

SUBMITTED BY Complete if applicable

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Signature				Date	20 Nov 2000

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PU 000125/RCA 89,324

SERIAL COMPRESSED BUS INTERFACE HAVING A REDUCED PIN COUNT

1. Technical Field

The present invention relates generally to digital data
5 communications and, in particular, to a serial compressed
bus interface having a reduced pin count.

2. Background Description

Conventional serial compressed data buses are dedicated
10 to a single compressed data stream. Moreover, such buses
require at least 3 to 4 pins. A typical 3 wire interface
consists of a serial data signal, a clock signal and a sync
or framing signal. The data is delivered in packets that
are of a fixed size and the first bit of a packet is
15 indicated by driving the sync or frame signal active.

An alternate 3 wire interface replaces the sync signal
with a valid signal. The valid signal indicates when data
is valid on the interface. As with the previous interface,
this interface also requires packets to be of a fixed
20 length. The first bit of a packet is indicated by driving
the valid signal active. The valid signal is then required
to remain active for the duration of a packet and is driven
low at the end of the packet. When the valid signal is
inactive, the data is ignored by the receiving device.
25 Since the active edge of the valid signal is used to
indicate the first bit of a packet, the valid signal must be
driven inactive for at least one bit time between packets.

A widely accepted serial transport interfaces uses 4

wires to deliver data, clock, sync and valid signals. Like the 3 wire interface, the sync signal is driven active to indicate the first bit of a packet. Similarly, the valid signal is used to identify when data is valid on the
5 interface. This approach gives the added flexibility that data gaps may exist within a packet time. Also, since the sync signal indicates the start of a new packet, there is no requirement for a gap between consecutive packets.

Given the current state of the art, there is a need for
10 a serial compressed data bus that delivers more than one single compressed data stream. Moreover, there is a need for a serial compressed data bus interface having a reduced number of pins with respect to that required by conventional serial compressed data buses.

15

SUMMARY OF THE INVENTION

The problems state above, as well as other related problems of the prior art, are solved by the present invention, a serial compressed bus interface having a
20 reduced pin count.

The invention advantageously reduces the pin count associated with conventional serial compressed buses by time-division multiplexing a plurality of compressed data streams onto a shared data line. Moreover, the invention
25 advantageously encodes data valid and data request handshake signals rather than using a unique handshake signal pair for each compressed data stream as is done in conventional

serial compressed buses.

These and other aspects, features and advantages of the present invention will become apparent from the following detailed description of preferred embodiments, which is to 5 be read in connection with the accompanying drawings.

BRIEF DESCRIPTION OF THE DRAWINGS

FIG. 1 is a block diagram of a serial compressed bus and serial compressed bus interface, according to an 10 illustrative embodiment of the invention;

FIG. 2 is a diagram illustrating the encoding of the CB_DV[2:0] signal, according to an illustrative embodiment of the invention;

FIG. 3 is a diagram illustrating the encoding of the 15 CB_REQ[3:0] signals, according to an illustrative embodiment of the invention;

FIG. 4 is a timing diagram illustrating the timing relationship of some of the signals of the bus, according to an illustrative embodiment of the invention; and

20 FIG. 5 is a diagram illustrating some of the timing parameters of some of the signals of the bus, according to an illustrative embodiment of the invention.

DETAILED DESCRIPTION OF PREFERRED EMBODIMENTS

It is to be understood that the present invention may 25 be implemented in various forms of hardware, software, firmware, special purpose processors, or a combination thereof. Preferably, the invention is implemented as a

combination of hardware and software.

It is to be further understood that, because some of the constituent system components depicted in the accompanying Figures may be implemented in software, the
5 actual connections between the system components may differ depending upon the manner in which the present invention is programmed. Given the teachings herein, one of ordinary skill in the related art will be able to contemplate these and similar implementations of the present invention.

FIG. 1 is a block diagram of a serial compressed bus 100 and a serial compressed bus interface 199, according to an illustrative embodiment of the invention. In the illustrative embodiment, serial data enters an integrated circuit through the bus 100. The bus 100 is implemented
15 with a single serial data line that is time multiplexed between each of a plurality of data sources. Packet data from the different data sources is interleaved onto the single serial data line on byte boundaries. Each of the data sources is delivered to one or more data consumers in
20 the receiving application device. As used herein, the term Application@ refers to a consumer or processor of a compressed data stream, such as, for example, an MPEG2 video decoder or an AC-3 audio decoder.

To support decoding and presentation of multiple concurrent audio and video streams, the bus 100 will have support for up to seven separate application decoders. That is, the bus 100 can deliver seven compressed data streams

corresponding to seven application decoders. It is to be appreciated that while the illustrative embodiment of FIG. 1 shows the use of seven compressed data streams the invention is not so limited and, thus, any feasible number of
5 compressed data streams may be employed in accordance with the invention, while maintaining the spirit and scope thereof.

In the current state of the art, seven compressed data streams would be delivered over seven compressed data
10 interfaces. Each of these interfaces would normally consist of at least three signals, requiring a total of 21 signals for seven compressed data streams. According to the invention, the bus 100 delivers the seven compressed data streams through nine external signals: CB_CLK; CB_DATA;
15 CB_DV[2:0]; and CB_REQ[3:0]. The pin count of the bus 100 is reduced by a time-division multiplexing of the seven compressed data streams onto a shared data line. The pin count of the bus 100 is also lowered by encoding DV (data valid) and REQ (data request) handshake signals rather than
20 using a unique handshake signal pair for each compressed data stream.

The bus 100 includes the following five inputs: CB_CLK; CB_DATA; and CB_DV[2:0]. The CB_CLK signal is the compressed bus serial clock, which supports a maximum speed
25 of 100MHz. The CB_DATA signal is the compressed bus serial data, which is valid on the rising edge of CB_CLK. The CB_DV[2:0] signals indicate that data on CB_DATA is valid

for one of the seven supported application devices.

Each of the BUF_FULL[6:0] signals represents a compressed data buffer. It is to be appreciated that the phrase Acompressed data buffer@ and the term AFIFO@ (First-In-First-Out) are used interchangeably herein. When one of the BUF_FULL[6:0] signals is set to A1", it indicates that the corresponding compressed data buffer is full and cannot accept more data.

The bus 100 includes the following output: CB_REQ[3:0].
10 The CB_REQ[3:0] signals correspond to a request from at least one of the application devices.

Each of the BUF_SEL[6:0] signals represents an application device. When one of the BUF_SEL[6:0] signals is set to A1", it indicates that data will be removed from the
15 application specific FIFO and sent to a common transport demultiplexing circuit 150.

A bus interface circuit 199 includes a serial-to-parallel converter 110, enable logic 112, and a request control circuit 114. The bus interface circuit 199 is
20 coupled to a plurality of compressed data buffers 130-136 which, in turn, are coupled to main memory through a multiplexor 140 and transport de-multiplexor 150. Signals from the converter 110, enable logic 112, and the request control circuit 114 are used to write to the plurality of
25 compressed data buffers 130-136.

The serial-to-parallel converter 110 converts serial data to parallel data. The serial data is time-division

multiplexed and is input by the CB_DATA signal. The parallel data is 8-bits (1-byte) wide and is output by the CDATA signal. The CDATA signal is provided to the plurality of compressed data buffers 130-136.

5 The enable logic 112 selects a particular compressed data buffer to which data is to be written, based on the CB_DV[2:0] signal input thereto. Accordingly, the enable logic 112 outputs the BUF_SEL[6:0] signals.

The request control circuit 114 inputs the
10 BUF_FULL[6:0] signals and outputs the CB_REQ[3:0] signals. Thus, the request control circuit 114 indicates when one or more of the compressed data buffers 130-136 is full and, thus, no additional data can be written thereto.

As noted above, the CB_DV[2:0] signals are used to
15 indicate that valid data is present on CB_DATA for one of the seven application FIFOs 130-136. FIG. 2 is a diagram illustrating the encoding of the CB_DV[2:0] signal, according to an illustrative embodiment of the invention. The encoding has been chosen such that an external IC that
20 supports three separate strobe signals to strobe data into the video decoder could be made to work with the bus 100 and still support two compressed video streams and one compressed audio stream. The CB_DV[2:0] signals will change state on the rising edge of the CB_CLK signal. The
25 CB_DV[2:0] signals will hold a state for a minimum of eight CB_CLK cycles and a multiple of eight CB_CLK cycles. The data present on the CB_DATA signal can only be valid for one

application FIFO at a time.

As noted above, the serial data for each application is converted into byte wide parallel format and transferred to the appropriate compressed data buffer. There is one FIFO (one of FIFOs 130 though 136) implemented for each application device. It is to be appreciated that the aggregate data rate received for all application devices should not exceed the sum total of the maximum data rate of all of the input channels.

The CB_REQ[3:0] signals are used to request compressed data for each of the application devices 130-136. When there is space available in an application=s FIFO, the corresponding CB_REQ line will be driven high. When there is no space available in an application=s FIFO, the corresponding CB_REQ line will be driven low. Several of the CB_REQ[] lines may be high at the same time.

In the illustrative embodiment of this invention, CB_REQ[3:0] can uniquely identify requests for data from as many as four unique application devices. In this embodiment it is to be understood that four of the application devices are grouped such that they share a single CB_REQ line. However, it is to be appreciated that the invention does not require any specific grouping of application devices or sharing of CB_REQ lines among application devices. Given the teachings of the invention provided herein, one of ordinary skill in the related art would readily contemplate a different grouping of application devices to share the

available CB_REQ lines, or implementations of the invention that allow a request from each application device to be uniquely identified. FIG. 3 is a diagram illustrating the encoding of the CB_REQ[3:0] signals, according to the

5 illustrative embodiment of the invention.

The CB_REQ[1] signal maps to the PIP/record channel video. It is possible within a system for multiple videos to be present on a single broadcast transponder. To allow the simultaneous decode of up to four videos present on a
10 single transponder, the CB_REQ[1] signal is actually mapped to four separate compressed data buffers. When all of the compressed data buffers mapped to the CB_REQ[1] signal are ready to accept data, then the CB_REQ[1] signal is driven high. If any of the buffers mapped to the CB_REQ[1] signal are not ready to receive data, then the CB_REQ[1] signal is held low. If the data carried by the transponder is not multiplexed in a way that will allow simultaneous video
15 decode of all videos present, then it is possible to underflow one or more of the bit buffers serviced by
20 CB_REQ[1]. No provision will be made in this block to recover from this condition. However, given the teachings of the invention provided herein, one of ordinary skill in the related art will readily contemplate various modified configurations of the bus 100 which maintain the spirit and
25 scope of the invention while allowing for recovery from underflow conditions. FIG. 4 is a timing diagram illustrating the timing relationship of some of the signals

of the bus 100, according to an illustrative embodiment of the invention. FIG. 5 is a diagram illustrating some of the timing parameters of some of the signals of the bus 100, according to an illustrative embodiment of the invention.

5 Although the illustrative embodiments have been described herein with reference to the accompanying drawings, it is to be understood that the present system and method is not limited to those precise embodiments, and that various other changes and modifications may be affected
10 therein by one skilled in the art without departing from the scope or spirit of the invention. All such changes and modifications are intended to be included within the scope of the invention as defined by the appended claims.

WHAT IS CLAIMED IS:

1. A serial compressed bus interface, comprising:
a serial-to-parallel converter having a single serial
5 data input line adapted to receive time-division multiplexed
serial data from a plurality of data sources; and
enable logic adapted to input at least one data valid
signal that identifies each of a plurality of data consumers
for which the time-division multiplexed serial data is
10 valid.

2. The serial compressed bus interface according to
claim 1, wherein said serial-to-parallel converter is
further adapted to convert the time-division multiplexed
15 serial data to parallel data, and to output the parallel
data to the plurality of data consumers.

3. The serial compressed bus interface according to
claim 1, further comprising a request control circuit
20 adapted to output at least one request signal that requests
the time-division multiplexed serial data for at least one
of the plurality of data consumers.

25 4. The serial compressed bus interface according to
claim 3, further comprising at least one encoder adapted to
encode at least one of the at least one data valid signal

and the at least one request signal to correspond to more than one of the plurality of data consumers.

5. The serial compressed bus interface according to
5 claim 3, wherein the request control circuit is further adapted to encode the at least one request signal to correspond to more than one of the plurality of data consumers.

10 6. A method for transmitting serial compressed data from a plurality of data sources to a plurality of data consumers, comprising the steps of:

time-division multiplexing the serial compressed data from the plurality of data sources to generate time-division
15 multiplexed serial compressed data; and

transmitting the time-division multiplexed serial compressed data to the plurality of data consumers.

7. The method according to claim 6, wherein said
20 transmitting step transmits the time-division multiplexed serial compressed data on a single data line.

8. The method according to claim 6, further comprising the step of encoding a data valid signal to
25 indicate that the time-division multiplexed serial compressed data is valid for more than one of the plurality of data consumers.

9. The method according to claim 6, further comprising the step of encoding a request signal to indicate that the time-division multiplexed serial compressed data is
5 requested by more than one of the plurality of data consumers.

10. A method for transmitting serial compressed data from a plurality of data sources to a plurality of data
10 consumers, comprising the steps of:

interleaving serial compressed packet data from the plurality of data sources to generate time-division multiplexed serial compressed data; and

15 transmitting the time-division multiplexed serial compressed data to the plurality of data consumers.

COMPRESSED SERIAL BUS

Abstract

There is provided a serial compressed bus interface
5 having a reduced pin count. The interface includes a
serial-to-parallel converter having a single serial data
input line adapted to receive time-division multiplexed
serial data from a plurality of data sources. Enable logic
is adapted to input at least one data valid signal that
10 identifies each of a plurality of data consumers for which
the time-division multiplexed serial data is valid.

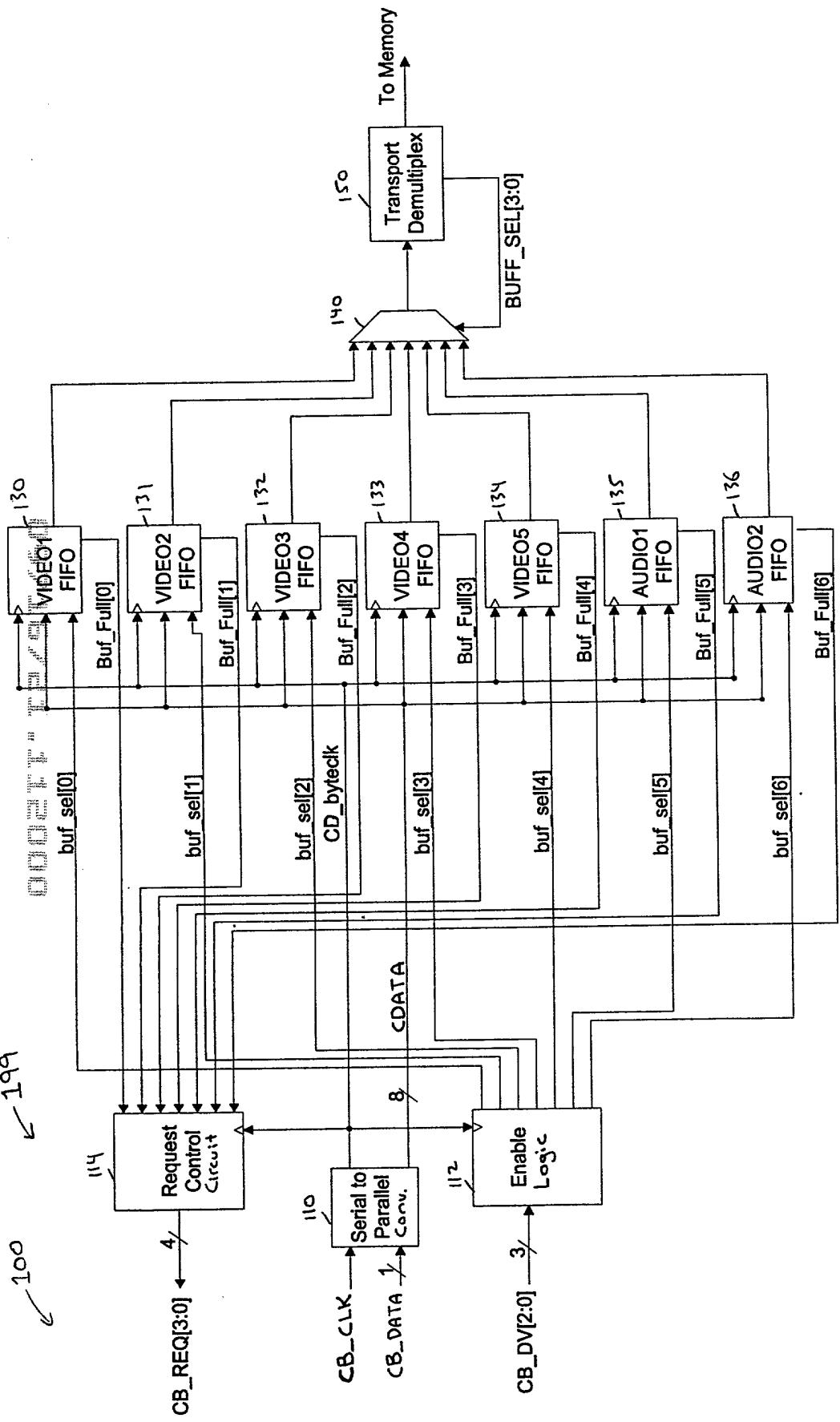


FIG. 1

CB_DV[2:0]	Application Buffer
000	No Data
001	Video1
010	Video2
011	Audio2
100	Audio1
101	Video3
110	Video4
111	Video5

FIG. 2

CB_REQ[3:0]	Requesting Application
0000	No requests
xxx1	Video1
xx1x	Video2/PIP
x1xx	Audio1
1xxx	Audio2

FIG. 3

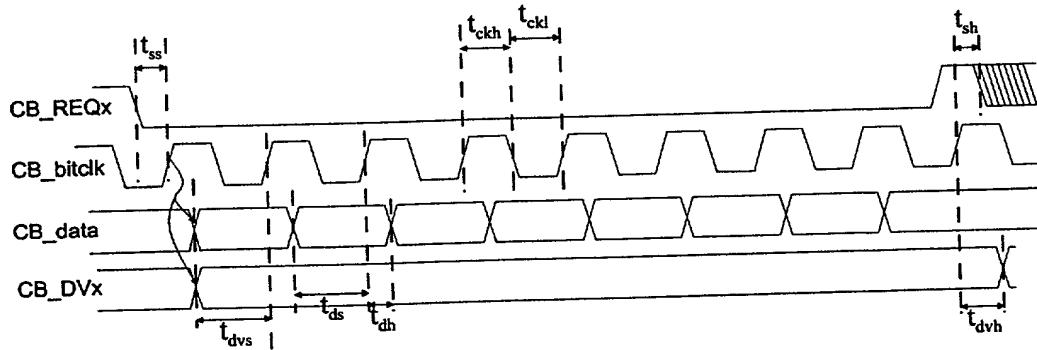


FIG. 4

0 9 8 7 6 5 4 3 2 1

Parameter	Description	Min	Typ	Max	Units
T_{ss}	Setup of CB_REQx before rising edge of CB_bitclk				ns
T_{sh}	Hold time of CB_REQx after rising edge of CB_bitclk				ns
T_{dvs}	Setup of CB_DVx before rising edge of CB_bitclk				ns
T_{dvh}	Hold time of CB_DVx after rising edge of CB_bitclk				ns
T_{ds}	Setup of CB_data before rising edge of CB_bitclk				ns
T_{dh}	Hold of CB_data after rising edge of CB_bitclk				ns
T_{ckh}	High time of CB_bitclk	5			ns
T_{cki}	Low time of CB_bitclk	5			ns

FIG. 5